A novel solid-state self powered neutron detector

Nicholas LiCausi*[a], Justin Dingley[b], Yaron Danon[b], Jian-Qiang Lu[a] and Ishwara B. Bhat+[a]

[a]Department of Electrical, Computer and Systems Engineering,
[b]Department of Mechanical, Aerospace and Nuclear Engineering,
Rensselaer Polytechnic Institute, 110 8th Street, Troy, NY USA 12180-3522

ABSTRACT

Detection of nuclear materials is critical in preventing traffic of illicit nuclear materials. Several methods that are based on detection of spontaneous or induced emission of fission neutron are considered. Efficient fast and thermal neutron detectors are generally required. For some applications these detectors must have fast response and should be deployed with large or small detection area.

This work expands upon the basic concept of coating a p-n junction solar cell with a neutron detection layer that typically employs either ^{6}Li or ^{10}B. ^{10}B has a larger absorption cross section and results in higher detection efficiency. When an incident neutron interacts with ^{10}B, it releases an α-particle and a ^{7}Li ion; this α-particle excites electron-hole-pairs in the silicon p-n junction. This work investigated a variety of different silicon trench/pillar/hole geometries in combination with the ^{10}B filling or coating; thermal neutron detection efficiencies as high as 30% are projected. It utilizes trenches spaced as closely as 2 μm and 50 μm deep. Simulations predict that when these single layer detectors are bonded in a multiple layer configuration, efficiencies in the range of 90% could be achieved.

Along with nuclear and electrical simulations, a highly controllable deep-reactive-ion-etching (DRIE) recipe is developed for trench/pillar/hole etching. The ability to create p-n junctions along those trenches is presented. Trenches and pillars as small as 2 μm by 2 μm are fabricated and p-n junctions are created along their surface. Smooth, uniform trenches are ready for trench refilling procedures.

Keywords: Neutron detector, thermal neutrons, solid-state detector, DRIE, computer simulations

1. INTRODUCTION

The threat of nuclear materials is on the rise as sources of material increase. It is therefore important to have an effective and efficient neutron detector to detect and prevent the proliferation of illicit nuclear materials. However, having a detector that boasts high efficiencies is not enough. The detector needs to be small, lightweight, portable, and low cost. Studies conducted have shown that as the number of detectors positioned at countries' borders increase, the overall likelihood of stopping a would-be terrorist also increases.

With these issues in mind, research has begun in the area of making a low cost, portable, and still highly efficient neutron detector. Such a detector may not require an external voltage source and could be entirely self-powered. With no moving parts it would be robust and work in a variety of different environments. Furthermore the device simplicity makes it easily scalable and can be employed for a variety of uses.

The basic principle of operation involves a solar-cell-like p-n junction and an activation material [1]. This work uses silicon to create the solar-cell-like p-n junction and ^{10}B as the activation material. When an incident neutron interacts with a ^{10}B atom, it releases an alpha (α) particle and a ^{7}Li ion. These α particles lose energy due to ionizing collisions, creating electron-hole pairs in the solar-cell-like material, allowing for electrical output from the detector.

* licaun@rpi.edu; www.rpi.edu/~licaun
+ bhati@rpi.edu; phone 1.518.276.2786; fax 1.518.276.6261

Hard X-Ray, Gamma-Ray, and Neutron Detector Physics X, edited by Arnold Burger, Larry A. Franks, Ralph B. James,
Proc. of SPIE Vol. 7079, 707908, (2008) · 0277-786X/08/$18 · doi: 10.1117/12.797036

The presented work highlights a method to increase the effective surface area of the detector. This method has been shown to increase efficiency, but is limited by geometrical effects [2]. This limit could be overcome by the photolithographic patterning of ambitious detector geometries and the use of deep reactive ion etching (DRIE).

In this work, various detector structures are designed and simulated. Initial efficiency calculations using GEANT4 explores the geometrical effects of various designs. Detector structures are simulated to further prove critical theories of detector operation before proceeding with the fabrication. In addition, fabrication steps are simulated with a variety of software packages to aid in process development. Following the design and simulation, fabrication and trench etching and refilling steps are designed and investigated.

2. SIMULATIONS

A variety of different simulation programs were used to optimize the detector design. For the nuclear physics and neutron / boron / alpha particle interaction portion of the device GEANT4 [3] was used and is discussed first. For the electrical carrier transport analysis, MEDICI [4], a semiconductor simulation program, was used, with several design parameters analyzed.

2.1 Nuclear Interaction Simulation

Optimization of the parallel trench design was accomplished in three steps: determination of the optimization parameters, analytical calculation of initial parameter values for simulation, and iterative Monte Carlo simulations to find optimal parameter values.

2.1.1 Optimization Parameters

There are three main factors that affect detection efficiency, the first of which is neutron absorption probability. This can be calculated by the following equation

$$P(x) = 1 - e^{-\Sigma_a \cdot x_D}$$
$$\Sigma_a = \sigma_a \cdot N \tag{1}$$

where Σ_a and σ_a are the energy dependent macroscopic and microscopic cross-sections of the absorber, respectively, N is the number density of the material, and x_D is the neutron path length. Using ^{10}B as the absorber and assuming thermal neutrons (E = 0.0253 eV) incident perpendicular to the surface of the absorber, the absorption probability is simply a function of the material depth x_D.

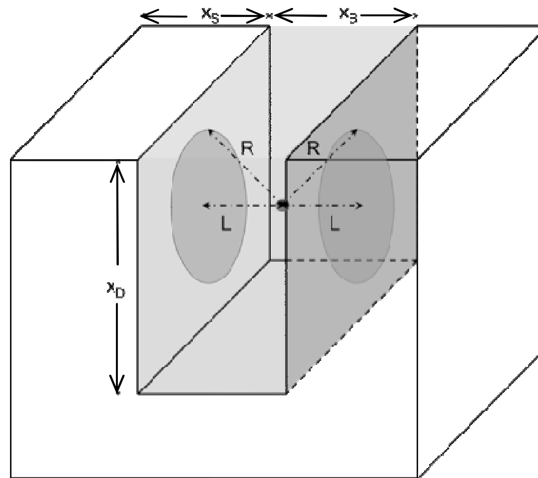


Fig. 1. Simplified device schematic of the trenched device showing the boron filled trench, silicon fin, and the effective area of incidence of the alpha particle.

The volume fraction of absorber in the detector is the second factor that affects detection efficiency. For a parallel trench device, this geometric factor is found by

$$F = \frac{x_B}{x_B + x_S} \tag{2}$$

where x_B is the width of each trench and x_S is the width of each wall (Fig. 1).

The last factor affecting detector efficiency is the ability of the charged particles resulting from neutron interaction in the absorption layer to escape into the silicon. The particles must have a minimum energy upon reaching the silicon to allow for adequate electron-hole pair collection, which in this case was arbitrarily set at 200 keV. The dominant nuclear reaction (94%) when a neutron is absorbed by ^{10}B is

$$^{10}B + n = \alpha + ^{7}Li + \gamma \tag{3}$$

where α= 1.47 MeV, ^{7}Li = 0.84 keV, and γ= 0.48 keV.

Given the above initial energies, while ensuring that the minimum energy required for detection is retained, the particles have maximum ranges of 2.9 µm and 1.48 µm in ^{10}B for the alpha particle and lithium ion, respectively. These ranges can then be used to calculate the acceptance solid angle for each particle according to the following equation

$$\Omega = 2\pi\left(1 - \frac{L}{\sqrt{L^2 + R^2}}\right) \tag{4}$$

where L is the distance from the reaction site to the closest wall and R is the maximum range of the particle. In order to calculate the probability of the particle reaching a wall, the solid angle must be multiplied by 2 to account for the second wall (Fig. 1). The isotropic nature of the particle emission, combined with interaction location being equally probable across the absorber, allows for the assumption that

$$L = \frac{x_B}{2} \tag{5}$$

such that the total probability of detection for each particle is given by

$$P(\Omega) = \frac{2\Omega}{4\pi} = \frac{2 \cdot 2\pi\left(1 - \frac{\frac{x_B^2}{2}}{\sqrt{\frac{x_B^2}{2} + R^2}}\right)}{4\pi} = 1 - \frac{\frac{x_B^2}{2}}{\sqrt{\frac{x_B^2}{2} + R^2}} \tag{6}$$

Combining equations (1), (2) and (6) results in an overall detector efficiency of

$$P = \left(1 - e^{-\Sigma_a \cdot x_D}\right)\left(\frac{x_B}{x_B + x_S}\right)\left(1 - \frac{\frac{x_B^2}{2}}{\sqrt{\frac{x_B^2}{2} + R^2}}\right) \tag{7}$$

which, for a given interaction material, is dependent only on the layer depth, trench width, and wall thickness. It should be noted that the above equation assumes that every charged particle reaching the silicon wall deposits sufficient energy to be detected.

Equation (7) was then used to calculate the initial parameter values for the Monte Carlo simulation. To accomplish this, the incident neutron energy was set at 0.0235 eV, ^{10}B was used as the absorber, trench depth (x_D) was fixed at 30 µm, and wall thickness (x_S) was set to 2 µm. After performing calculations, it was determined that the optimum trench widths were ~2 µm for alphas and ~1.75 µm for ^{7}Li ions. After substitution of these values into equation (7), it could be seen that decreasing the value of x_S would result in an increasing detector efficiency. This indicated that there existed no optimal wall thickness for any given trench width. As such, the initial wall thickness was arbitrarily set to 2 µm.

2.1.2 Monte Carlo Simulations

The GEANT4 Monte Carlo toolkit [3] was the simulation software utilized due to its ability to accurately transport and track alpha particle and light ion energy deposition in the detector. The following are the simulation parameters:

- Pure silicon (monocrystalline) detector material
- Enriched boron (99% ^{10}B) trench material
- 5 mm x 5 mm x 50 µm detector size
- 20 µm base depth
- 30 µm trench depth
- Varying trench and wall widths
- 1,000,000 neutrons incident on detector per simulation
- 200 keV minimum energy deposition per neutron

A total of 60 simulations were run, starting with the trench width and wall thicknesses determined from the analytical calculations. The trench depth was set to 30 µm, while the trench thickness and wall thickness were varied.

As Fig. 2(a) shows, maximum detection efficiency of alpha particles per neutron, with a 200 keV cutoff, is ~37%. Optimal parameters at this efficiency are a trench width of 1.25 µm and a wall thickness of 0.8 µm. Detection efficiency of ^{7}Li ions, also with a 200 keV cutoff, is considerably lower at 22%, with a corresponding trench width of 1.25 µm and a wall thickness of 1.5 µm (Fig. 2(b)).

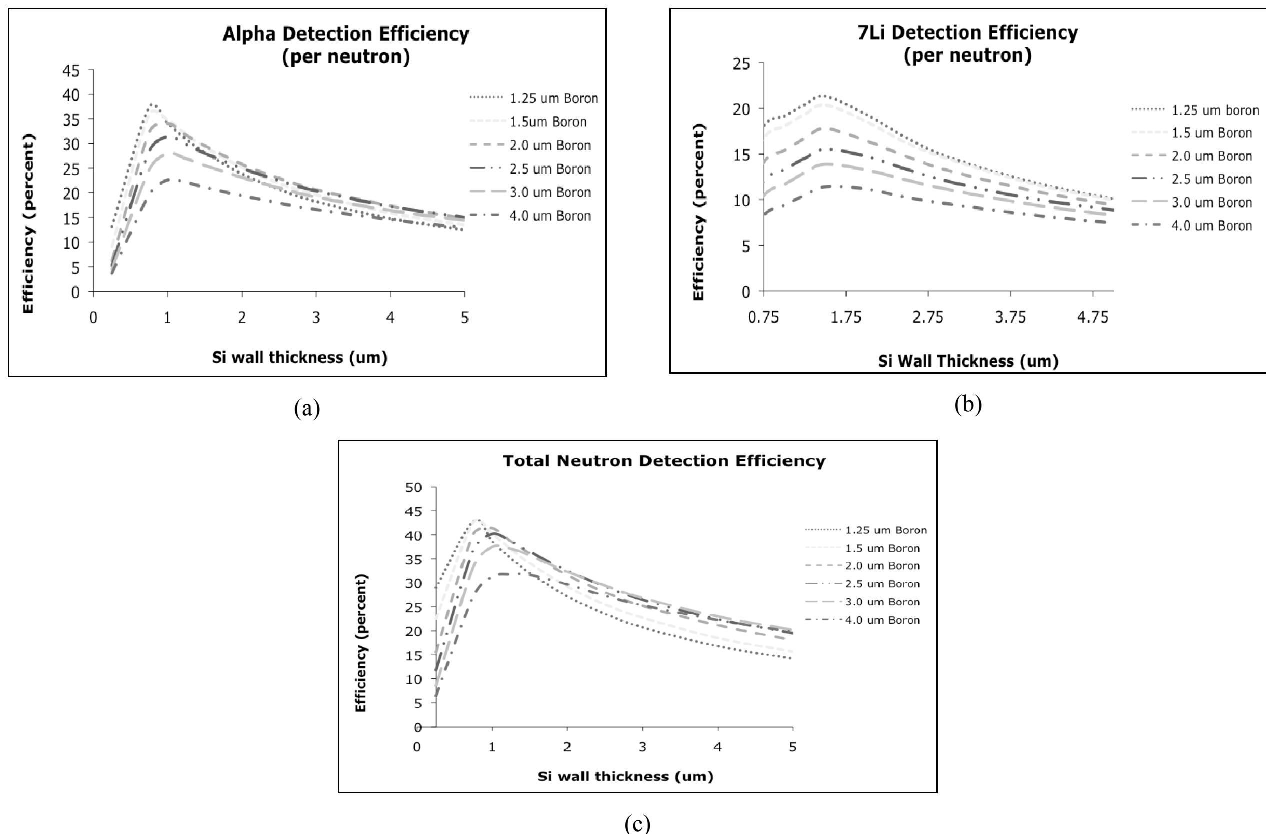


Fig. 2. (a)Alpha detection efficiency per neutron and (b) ^{7}Li ion detection efficiency per neutron are both related to silicon wall thickness for different boron-filled trench widths ranging from 1.25 µm to 4.0 µm. These values are both used to find the (c) total neutron detection efficiency, shown as a function of pillar and trench width.

Total neutron detection efficiency (Fig. 2(c)), which has a total energy deposition ($\alpha + {}^{7}Li$) of 200 keV, has a maximum value of 43%. The corresponding trench width and wall thickness are 1.5 µm and ~1 µm, respectively. The increase in efficiency of 7% over alpha detection indicates that energy deposition in the detector from the lithium ions is non-negligible.

2.2 Detector Electrical Characteristics Analysis

MEDICI is a semiconductor simulation software that allows for the two dimensional simulation of a variety of semiconductor devices including MOS, JFET, p-n junction diodes and others. It has been designed for sub-micron or larger devices and has the ability to analyze devices with both multiple or single carrier dominated characteristics [4].

2.2.1 Depletion Layer and Capacitance Simulations

When designing the detector it is critical to take into account the device capacitance. Many detectors, including the design developed, detect the charge imparted by a particle or many particles and hence minimizing capacitance is important. The importance can be seen in the relationship described in equation (8) between voltage (V), capacitance (C), and the imparted charge (Q).

$$V = \frac{Q}{C} \tag{8}$$

In order to predict the capacitance for different device designs, it is important to understand the behavior of depletion layers in p-n junctions. A p-n junction, or the junction between p-type semiconductor and n-type semiconductor, forms a region that is depleted of free carriers and is therefore called the depletion region. This region maintains what is known as a built-in voltage. This voltage is dependant on the type of semiconductor and the doping concentrations of both the n-type and p-type materials. The relationship is shown below in equation (9),

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{9}$$

where k is the Boltzman constant, q is the electron charge, T is temperature in Kelvin, N_A is the p-type dopant concentration, N_D is the n-type dopant concentration, and n_i is the intrinsic carrier concentration for the given semiconductor at a particular temperature.

The built-in voltage in turn is used to calculate the width of the depletion region both on the n-type side and p-type side. This is given for the n-type side in equation (10),

$$X_n = \left[\frac{2K_S\varepsilon_o}{q}\left(\frac{N_A}{N_D(N_A + N_D)}\right)V_{bi}\right] \tag{10}$$

where K_S is the relative dielectric constant for the semiconductor (11.7 for Si) and ε_o is the dielectric permittivity of free-space. Similarly, the equation (11) gives the width of the depletion region on the p-type side of the junction.

$$X_p = \left[\frac{2K_S\varepsilon_o}{q}\left(\frac{N_D}{N_A(N_D + N_A)}\right)V_{bi}\right] \tag{11}$$

The sum of these two yields the depletion layer width, given by equation (12).

$$W_{dep} = X_p + X_n \tag{12}$$

This in turn allows for the calculation of the capacitance of the device through equation (13). It should be noted that this equation is generic for a given area with a constant depletion width.

$$C_{UNIT} = \frac{\varepsilon_{Si} A}{W_{dep}} \tag{13}$$

Further evaluation of the device reveals that if the pillar width and doping concentrations are properly manipulated, the pillar can be fully depleted. If the pillar width is smaller than double the depletion width, the depletion layer from each side of the pillar will meet, and therefore the entire pillar will be depleted of carriers. This condition is ideal because the

effective depletion layer width becomes the height of the pillar in the region of the pillar. In the region of the trench it remains the same as a planar device's depletion width.

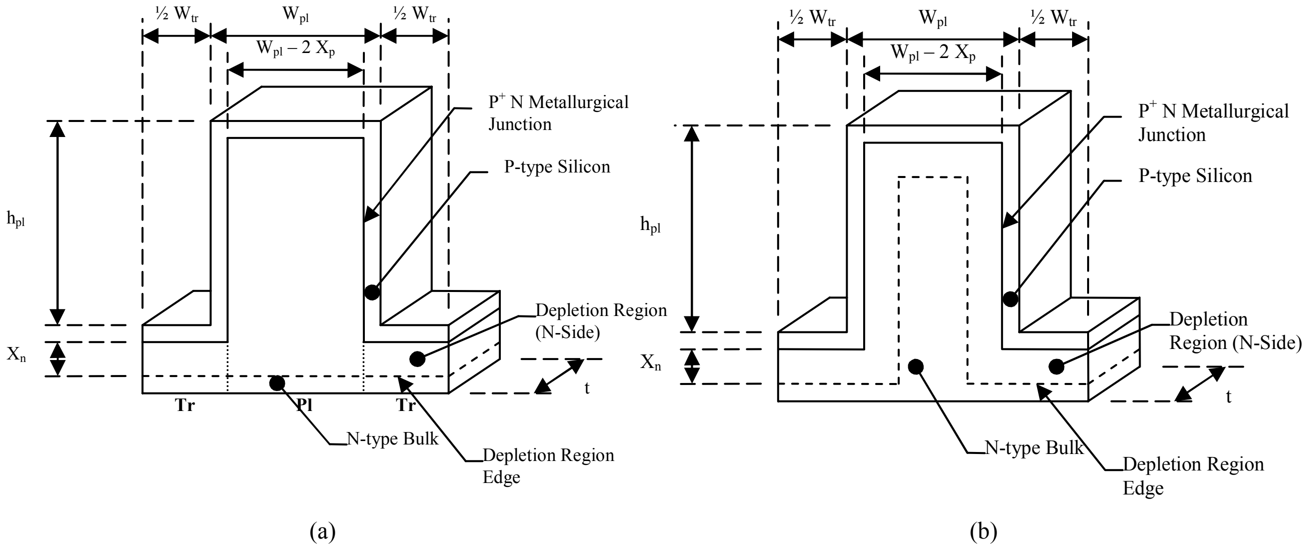


Fig. 3. (a) The fully depleted pillar schematic is shown. Capacitance is minimized when the pillar is fully depleted. (b) The partially depleted pillar schematic is not optimal because the effective surface area of the p-n junction is increased proportionally to the depth of the trenches.

In the context of Fig. 3(a), the generic capacitance equation shown above in equation (13) can be manipulated for this device to form equation (14). This equation assumes that the pillar and trench width are held constant as is typical with device designs that attempted to date.

$$\frac{Cap}{Area}=\frac{C_{UNIT}}{A_{UNIT}}=\frac{11.8\times 8.85\times 10^{-14}}{\left(W_{tr}+W_{pl}\right)}\left[\frac{W_{tr}}{W_{dep}}+\frac{\left(W_{pl}-2\ X_{p}\right)}{\left(W_{dep}+h_{pl}\right)}\right]F\ \cdot cm^{-2} \tag{14}$$

However, in a partially depleted scenario, the capacitance of the device increases tremendously. This is due to the large increase in effective area while maintaining the same depletion layer width. As shown in equation (13), it is ideal to have a fully depleted pillar to minimize capacitance. The depletion region travels along the entire surface of the pillar and trench. This can increase the effective surface area by 100 times the original if the pillars are on the order of 50 μm tall and are spaced 2 μm apart. In Fig. 3(b) the concept that lead to equation (15) is illustrated.

$$\frac{Cap}{Area}=\frac{C_{UNIT}}{A_{UNIT}}=\frac{11.8\times 8.85\times 10^{-14}\cdot\left(W_{tr}+W_{pl}+2h_{pl}\right)}{W_{dep}\cdot\left(W_{tr}+W_{pl}\right)}F\ \cdot cm^{-2} \tag{15}$$

According to theory, for a given doping and varying pillar/fin widths the capacitance should sharply drop when the doping is lowered below a given threshold.

2.2.2 Simulation Results

After considering the calculated capacitance and device characteristics with standard analytical calculations, these results were verified with the use of a UNIX-based software package named MEDICI [4]. This is a two-dimensional elemental and compound semiconductor simulation software that can handle a huge array of models and effects. In Fig. 4, shown below, the green represents n-Si, yellow represents p-Si and the light blue represents SiO_2. Although MEDICI is versatile, it does not have a parameter to model the behavior of pure boron and this is why SiO_2 was used instead. According to existing literature, it is anticipated that boron will behave as an insulator in pure form.

In Fig. 4 black lines and a red-dotted line are shown. The red dotted line represents the edge of the depletion region on the n-type side. Because the simulations held the doping concentrations constant ($N_A = 10^{18}$ cm^{-3} and $N_D = 10^{14}$ cm^{-3}), as the pillar width was decreased the edge of this depletion region gets closer together until at the 5 μm pillar and smaller the depletion region edges join. This is the most desirable situation, according to predictions.

After considering the predictions made by the hand calculations and the MEDICI capacitance simulated data, it seems that they collaborate well. The results of these simulations are plotted in Fig. 5. It is clear that the expected minimization of capacitance does take place as the depletion layer meets from each side of the pillar.

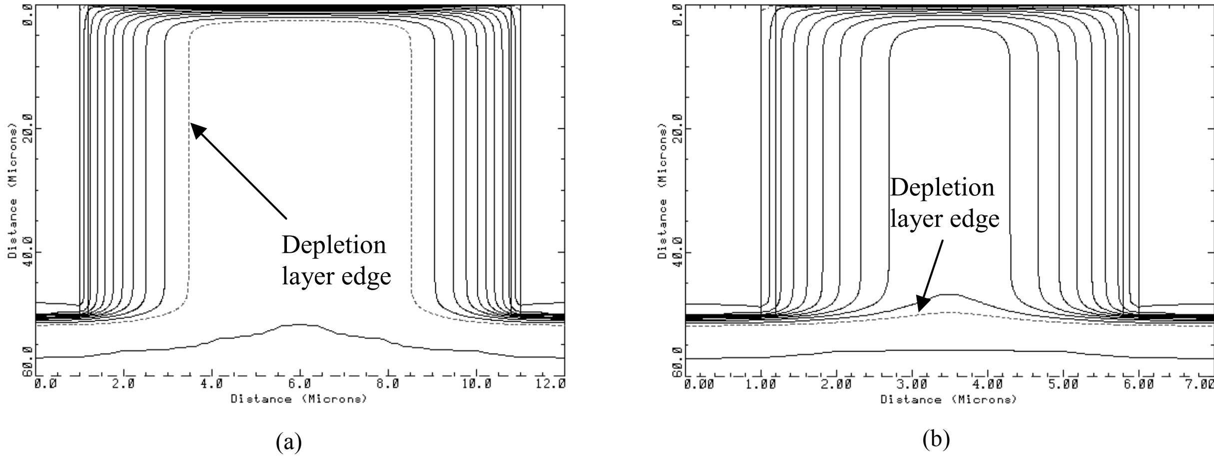


Fig. 4. MEDICI 2D simulations of (a) a 10 µm wide pillar of n-type silicon with a thin, continuous p-type layer on the surface of the pillar and trench and (b) a 5 µm wide pillar with the same n-type and p-type regions. If the pillar width is less than twice the n-side depletion region width, such as in (b) the pillar is fully depleted and the device capacitance is reduced.

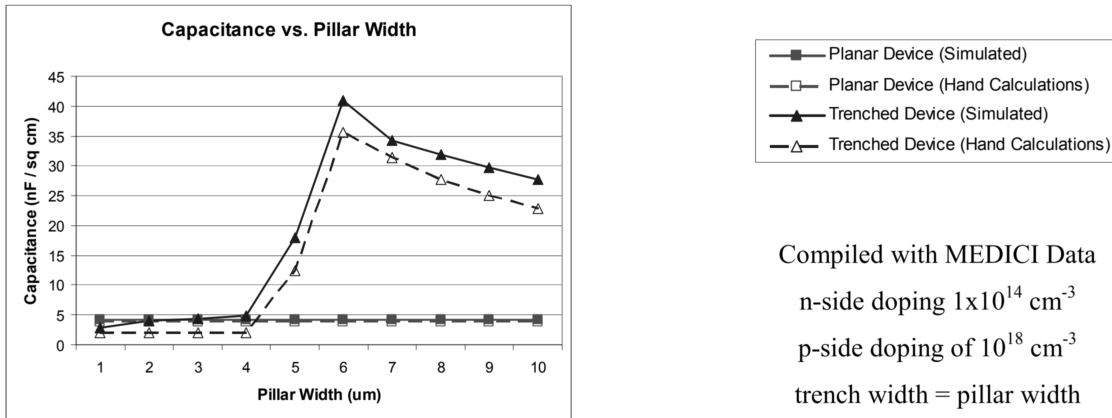


Fig. 5. Capacitance as a function of pillar width is shown to rise in the pillared structure until a threshold is met where the pillar width is less than or equal to twice the n-side depletion width.

3. DESIGN OF DETECTOR STRUCTURES

Many general design features have been considered with various simulations and calculations. Following this designing the actual physical mask set to produce the device utilized the simulations. It is important to allow spacing between the devices for dicing of the detectors after completion of the other processing steps. Although the ideal device may be an array of these smaller detectors, for testing purposes the detectors must be separated. This may not be necessary if 3D wafer level integration with pre-amplifiers is utilized.

Designing the devices was performed with Cadence [5]. In Fig. 6 schematic for the checkerboard, trench/fin, and hexagonal/honeycomb layouts are shown, respectively. Although these are not to scale, the basic patterns are the same and are produced at five different scales each. As simulated, the pillar and trench sizes were varied and include 2 µm, 4 µm, 5 µm, 6 µm and 8 µm in width. Because of the parallel nature of photolithography, all these design sizes are patterned and etched simultaneously.

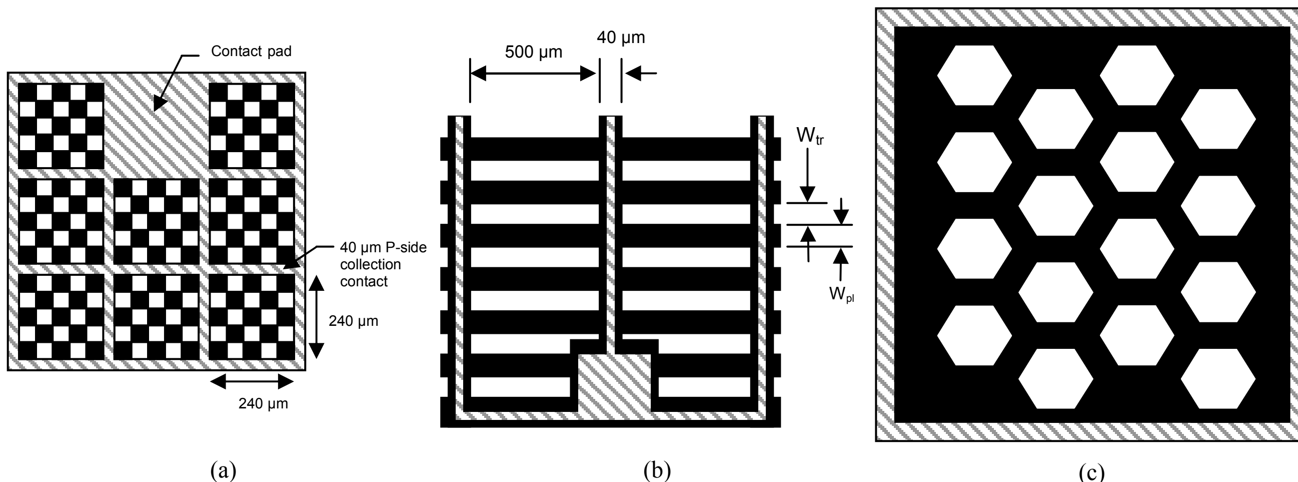


Fig. 6. This shows the (a) square/checkerboard configuration, (b) linear trench/fin configuration, and (c) a sub-cell of the hexagonal/honeycomb configuration. Some typical dimensions have been shown. The black represents un-etched silicon, the white represents etched or trenched silicon, and the hatched sections represent metal (Al) contacts.

4. FABRICATION CHALLENGES

4.1 Baseline Process Flow for Detector Fabrication

The processing can be broken down into 6 main stages that are shown below in Fig. 7. The first stage is the deposition and patterning of SiO_2. This is used as a diffusion barrier when depositing and annealing the boron. If this was not in place, the entire wafer would act as a single detector. Although this sounds ideal, detecting small neutron counts would be impossible due to a significantly larger capacitance. For this reason an array of smaller detectors is necessary.

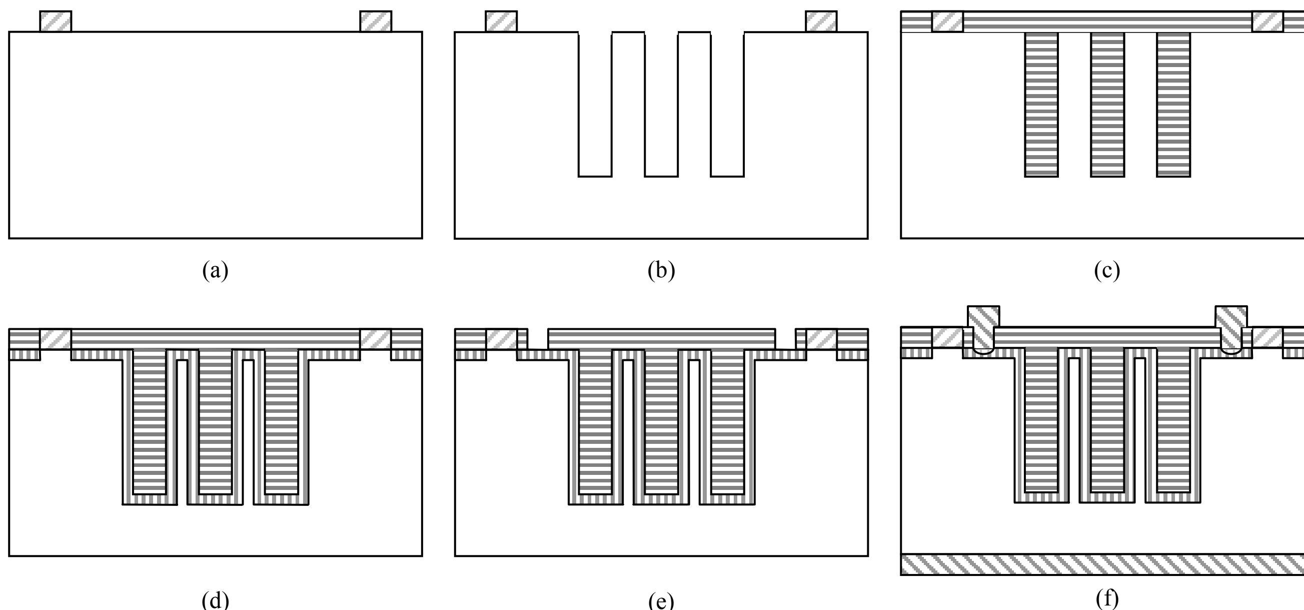


Fig. 7. There are 6 main stages that are shown in the above figure. (a) Stage 1: Starting with n-Si, SiO_2 is deposited & patterned to isolation regions. (b) Stage 2: Using the Bosch Process, the trenches/pillars are patterned & etched. (c) Stage 3: Trenches are filled with a boron containing substance. (d) Stage 4: Boron diffusion forms a continuous p-n junction. (e) Stage 5: Contact vias are etched into the boron containing film on the surface. (f) Stage 6: Metallization and form contacts.

The second stage, shown in Fig. 7(b), is the Deep Reactive Ion Etching (DRIE) stage. This patterning and etching is critical to the success of the detector. This process, also known as the Bosch process, allows for high aspect ratio, deep trench etching. The details of this process and its recipe development will be discussed further.

Following the creation of deep trenches, these trenches are filled with boron. This can be seen in Fig. 7(c). Although a variety of trench refilling methods have been proposed and studied, many of these methods yield nonuniform filling and can result in the presence of voids. For optimal detector efficiency, it is important to have as high a fill factor as possible. The use of Low Pressure Chemical Vapor Deposition (LPCVD) is considered. This uses diborane (B_2H_6) to deposit elemental boron [6]. Due to various safety requirements and chemical handling regulations, access to necessary materials to perform this LPCVD is difficult. Before proceeding to the next step, the boron is planarized in order to achieve a uniform thickness and more importantly, uniform lithography in the next stages of development.

Following boron deposition, a high temperature anneal is required. Following which, the detecting elements will all be in place. The last two sections are simply to pattern and etch contact vias (or holes) through the boron to the p-type silicon and then deposit and pattern the metal contacts on the front and back of the detector. The metal contacts are required in order to achieve a low-resistance ohmic contact. Upon completion of such a detector, electrical and detecting tests will begin.

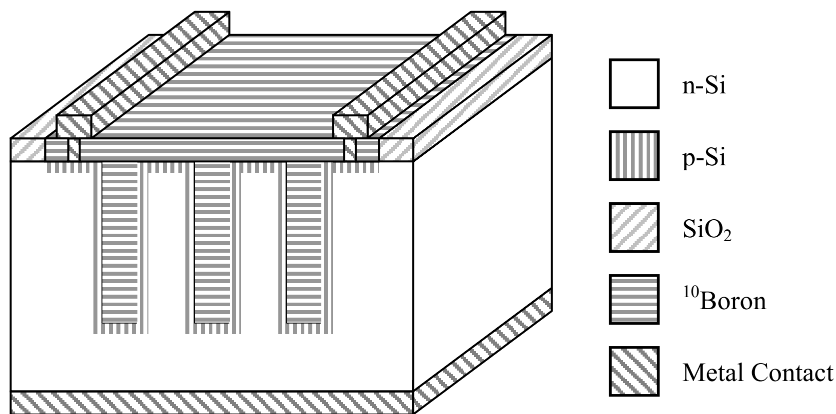


Fig. 8. 3D Cross-section view of the overall trench/fin neutron detector device schematic.

4.2 Deep Reactive Ion Etching

One of the most important steps in this process is the Deep Reactive Ion Etching (DRIE). This process was developed about fifteen years ago and is also known as the Bosch Process [7]. The basic idea of the process can be seen on the right side of Fig. 9 and consists of cycling between the deposition of a passivation layer (which coats the sidewalls as much as the horizontal surfaces) and then a silicon etching step. This alternation, if timed correctly can result in smooth vertical sidewalls with high depth to width aspect ratios. Aspect ratios as high as 30:1 have been achieved on 2 µm wide trenches that were 60 µm deep. Existing literature also reports aspect ratios as high as 50:1 or sometimes even greater.

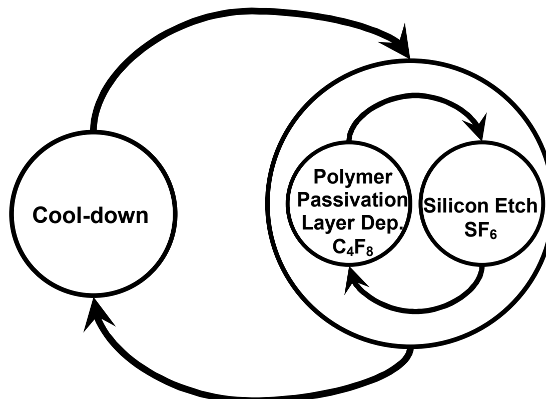
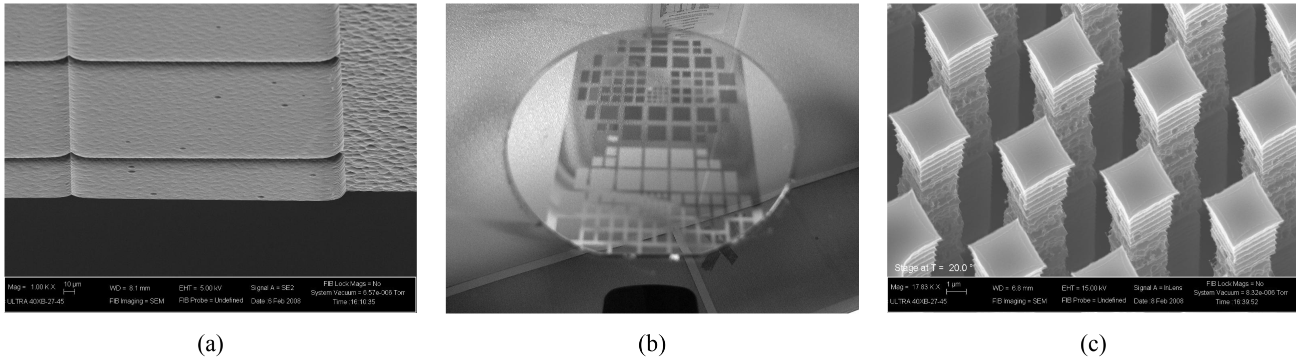


Fig. 9. The basic **D**eep **R**eactive **I**on **E**tching (DRIE) process cycle with a cool down stage.

4.2.1 Processing Issues and Results

Fig. 9 also shows a cool-down step in the process recipe. The cool-down step became necessary after some initial results suggested that the wafer was becoming so hot that the photo resist was burning off. Initially when the recipe was cycled for 8 minutes (necessary to achieve the desired depth of 50 μm) the wafer had no patterns left at all. This was observed with scanning electron microscopy and can be seen in Fig. 10(a).



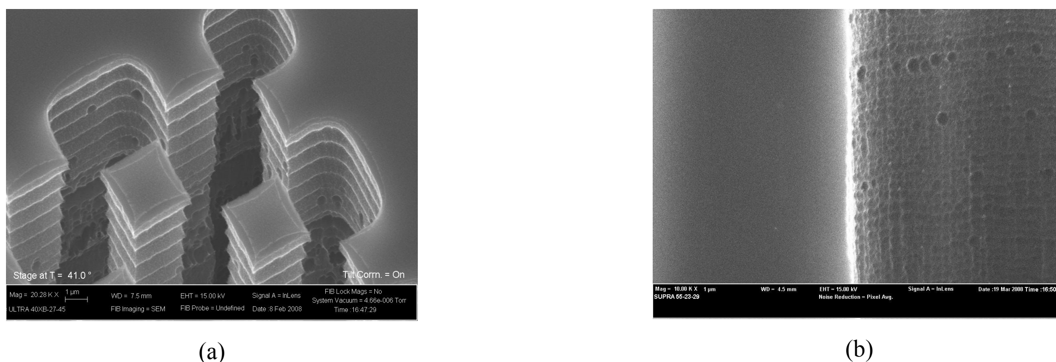
(a) (b) (c)

Fig. 10. There were a number of thermal issues during the process development of the DRIE process. Shown in the figure is (a) the total loss of the photo resist pattern as seen by scanning electron microscopy, (b) burning of some of the photo resist during individual etching size and (c) an observed non-uniformity with wafer depth caused by overheating during DRIE.

It was only after the total etching time was reduced did the problem become apparent. Only doing two minutes of etching/passivation cycles produced the burning that can be seen in Fig. 10(b). It is believed this was caused by non-uniformity in the application of thermal paste that was used to attach the smaller 3” wafer to the larger 8” wafer that is required for the plasma chamber to operate properly. It is this non-uniformity that lead to more burning in certain regions than others. The feasibility of using 8” wafers in future iterations is being reviewed.

After the cooling cycle was increased and a pattern was successfully etched into the silicon wafer it was reviewed with scanning electron microscopy. These results are shown in Fig. 10(c). Although this was great progress, the sidewall uniformity and smoothness was still not tolerable. It was concluded that the excessive pitting was due to minor overheating and the cooling cycle to etching/passivation cycle ratio was further increased to allow more time to cool between each etch. This increased the time to etch a given depth, but greatly increased the smoothness of the sidewalls.

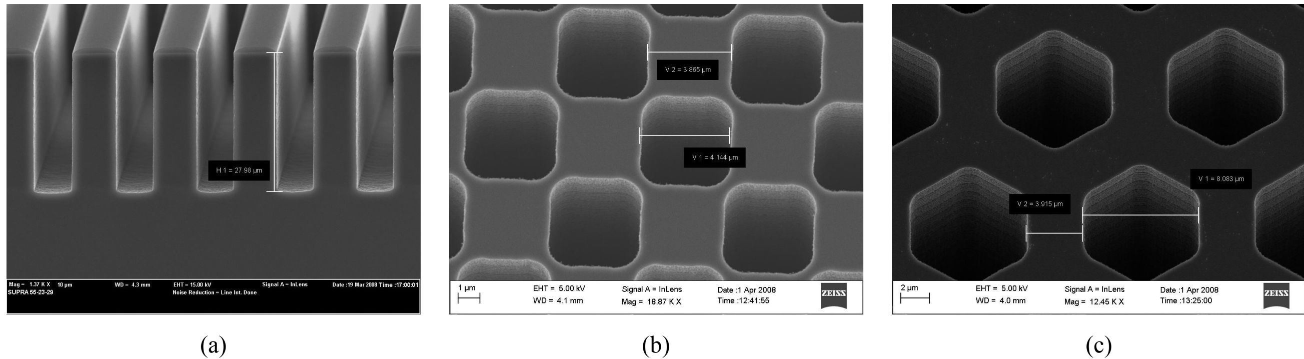
The last problem with the resulting etch profile was the existence of large scalloping on the sidewalls. This is due to the cyclical nature of the etching and passivation process. In order to make the scallops as small as possible, the time for each step of the cycle was reduced from 7 seconds of etching and 2 seconds of passivation deposition to 3.5 seconds and 1.5 seconds, respectively. This final modification to the recipe was effective and reduced the scallop size from roughly 1 μm in height to 200 nm in height. Likewise the depth into the sidewall of each scallop was also reduced proportionately. The scallop size before and after this recipe change are shown in Fig. 11(a) and Fig. 11(b), respectively.



(a) (b)

Fig. 11. A comparison of the an initial DRIE recipe and an optimized recipe with scanning electron microscopy show that (a) the sidewalls initially had large, deep scallops and then (b) were made smoother with much smaller, shallower scallops after reducing the etch and passivation cycle times.

After working with the aforementioned timing issues the DRIE process is now able to be finely tuned to deliver precisely controlled etching depths with various patterns with feature sizes as small as 2 µm. Below in Fig. 12(a-c) scanning electron microscopy shows trenches, checkerboard, and hexagonal patterns all etched with smooth, uniform sidewalls.



(a) (b) (c)

Fig. 12. Perfected patterning and DRIE recipes show that the process is capable of creating precisely designed geometries including (a) linear trenches or fins, (b) square holes or pillars in an interleaved or checkerboard configuration and (c) hexagonal holes or a honeycomb pattern.

4.3 Trench Refilling and Diffusion

As described in the previous sub-section, a lot of effort has been placed on etching smooth, uniform sidewalls when creating the trenches. This effort is to ensure that when filling the trenches with boron there are as few voids as possible. This is critical in order to create a uniform and continuous p-n junction along the bottom of the trench, sidewalls of the trench and top of the pillar. The p-region of the p-n junction is created by placing the wafer in an annealing furnace or Rapid Thermal Anneal (RTA) oven after the trench is filled with boron. The primary method to fill these trenches is LPCVD of diborane gas.

Some initial simulations have been performed using TSupreme4 [8], a UNIX-based software package. This high temperature anneal allows some of the boron that has filled the trenches to diffuse into the silicon walls and creates the necessary p-type silicon. The basic setup of the initial annealing simulation was to ramp the temperature slowly up to various peak temperatures over the span of 90 minutes. This is then followed by a 90 minute ramp down. Simulations of temperatures ranging from 600 °C to 1000 °C and times between 5 minutes and 60 minutes have been studied. The desired junction depth is between 100 and 200 nm. For this reason, a temperature of 880 °C for a time of 40 minutes is employed. This temperature and time combination was verified, also with TSupreme4.

Further experiments conducted with RTA of a boron spin-on-dopant [8] yield promising results. Preliminary results indicate a junction depth of 180 nm with p-region formation along the trench sidewalls. This alternate technique is however damaging to the silicon fins due to ultrasonic agitation of the sample in the dopant solution. This agitation is necessary to expel trapped gases from the trenches and allow the dopant to coat the surface. Further testing is necessary to fully characterize the p-n junction created using this method. The p-n junction formed along the trench/fin walls and has been verified with the use of a 4-point probe configuration. In the future equipment necessary for the LPCVD of diborane to refill the trenches should be operational and the process can be refined.

5. SUMMARY AND CONCLUSIONS

A novel solid-state self powered neutron detector is designed and simulated from a nuclear and semiconductor perspective by using GEANT4, MEDICI, TSupreme4, and other software packages. The simulated results agree with existing theoretical calculations. These results show than the optimal thickness of the silicon fins and the boron-filled trenches is 0.8 µm and 1.25 µm, respectively. The electrical simulations confirmed the critical theory that fully depleted pillars will result from pillar/fin widths narrower than twice the depletion width. This makes pillar/fin widths on the order of 5 µm or smaller necessary.

A DRIE process recipe is developed, producing well controlled pillars and trenches with smooth sidewalls. This is critical to the various trench refilling methods under investigation. Furthermore, with the continuous p-n junction

formation developed a variety of trench refilling methods are possible including LPCVD as described, electroplating, and boron carbide nanoparticles. The combination of the fabrication methods and new geometries investigated increases potential performance over existing designs substantially.

ACKNOWLEDGEMENTS

The authors would like to thank the support and input of the support staff of the Rensselaer Polytechnic Institute Micro-Nano-Clean-Room (RPI MNCR). This work is supported by the joint NSF/DNDO Academic Research Initiative, award number CBET-0736104.

REFERENCES

[1] C. Petrillo, F. Sacchetti, O. Toker, N. J. Rhodes, “Solid state neutron detectors”, Nucl. Instr. and Meth. in Physics Res. A, Vol. 378, 541-551, (1996).
[2] J. K. Shultis and D. S. McGregor, “Efficiencies of Coated and Perforated Semiconductor Neutron Detectors”, IEEE Transactions on Nuclear Science, Vol. 53, 3, (2006).
[3] S. Agostinell et al., “GEANT4—A Simulation Toolkit,” Nuclear Instruments and Methods in Physics Research Section A, Vol. 506, Issue 3, 250-303, (2003).
[4] Avant!, ”Medici, Two Dimensional Device Simulation Program”, User’s Manual, Version 2000.4, pp. lix, (2000).
[5] Cadence, “http://www.cadence.com/products/custom_ic/index.aspx”
[6] F. C. Eversteyn and B. H. Put, **“**Influence of AsH_3, PH_3, and B_2H_6 on the Growth Rate and Resistivity of Polycrystalline Silicon Films Deposited from a SiH_4–H_2 Mixture,” *Journal of the Electrochemical Society: Solid-State Science and Technology*, Vol. 120, No. 1, 106 – 110, (1973).
[7] F. Laermer, A. Urban and R. Bosch, “Milestones in Deep Reactive Ion Etching,” The 13th International Conference on Solid-State Sensors, Actuators and Microsystems, 2005, Vol. 2, 1118 – 1121, (2005).
[8] Synopsys, ”Taurus TSUPREM-4”, User Guide, Version Z-2007.3, (2007).
[9] Emulsitone, “Borofilm 100,” “http://www.emulsitone.com/”